L Number	Hits	Search Text	DB	Time stamp
1	9157	(stress adj2 test$3) or (burn-in adj2 test$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 11:23
2	1019	((stress adj2 test$3) or (burn-in adj2 test$3)) near5 (IC or (integrated adj2 circuit$1))	USPAT; EPO; JPO; DERWENT	2004/01/15 10:03
3	1154	((stress adj2 test$3) or (burn-in adj2 test$3)) near10 (IC or (integrated adj2 circuit$1))	USPAT; EPO; JPO; DERWENT	2004/01/15 10:03
4	830	((stress adj2 test$3) or (burn-in adj2 test$3)) near3 (IC or (integrated adj2 circuit$1))	USPAT; EPO; JPO; DERWENT	2004/01/15 10:03
5	149	(((stress adj2 test$3) or (burn-in adj2 test$3)) near3 (IC or (integrated adj2 circuit$1))) and (latch$2 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:24
6	418	(((stress adj2 test$3) or (burn-in adj2 test$3)) near3 (IC or (integrated adj2 circuit$1))) and (plurality or multiple near3 (latch$2 or flip-flop$1))	USPAT; EPO; JPO; DERWENT	2004/01/15 10:25
7	12	(((stress adj2 test$3) or (burn-in adj2 test$3)) near3 (IC or (integrated adj2 circuit$1))) and ((plurality or multiple) near3 (latch$2 or flip-flop$1))	USPAT; EPO; JPO; DERWENT	2004/01/15 10:29
8	121	(stress$3 near3 (IC or (integrated adj2 circuit$1))) and (latch$2 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:32
9	83	(stress$3 adj3 (IC or (integrated adj2 circuit$1))) and (latch$2 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:32
10	15	(stress$3 adj3 (IC or (integrated adj2 circuit$1))) same (latch$2 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:32
11	15	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) same (latch$2 or flip-flop$1)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:33
12	0	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and LSSD	USPAT; EPO; JPO; DERWENT	2004/01/15 10:36
13	0	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and ((scan adj2 design$1) or LSSD)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:36
16	0	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and (714/726.ccls.)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:38
17	0	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and (714/727.ccls.)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:38
14	3	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and ((scan adj2 test$3) or LSSD)	USPAT; EPO; JPO; DERWENT	2004/01/15 10:38
15	5	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and (714/724.ccls.)	USPAT; EPO; JPO; DERWENT	2004/01/15 11:06
18	0	(stress$3 adj3 (IC$1 or (integrated adj2 circuit$1))) and (714/!.ccls.)	USPAT; EPO; JPO; DERWENT	2004/01/15 11:07
19	21	((stress adj2 test$3) or (burn-in adj2 test$3)) and LSSD	USPAT; EPO; JPO; DERWENT	2004/01/15 13:12
20	972	(reduc$4 near5 current) near10 test$3	USPAT; EPO; JPO; DERWENT	2004/01/15 13:13
21	20	(reduc$4 near5 current) near10 ((stress or burn-in) adj4 test$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:14
22	52	(reduc$4 near5 current) same ((stress or burn-in) adj4 test$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:26

23	1279	((stress or burn-in or accelerat$4) adj4 test$3) near10 ((integrated adj2 circuit) or IC$2)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:28
24	956	((stress or burn-in or accelerat$4) adj2 test$3) near4 ((integrated adj2 circuit) or IC$2)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:50
25	869	((stress or burn-in) adj2 test$3) near4 ((integrated adj2 circuit) or IC$2)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:50
26	1	(((stress or burn-in) adj2 test$3) near4 ((integrated adj2 circuit) or IC$2)) same (reduc$5 near3 current)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:51
27	27	(((stress or burn-in) adj2 test$3) near4 ((integrated adj2 circuit) or IC$2)) and (reduc$5 near3 current)	USPAT; EPO; JPO; DERWENT	2004/01/15 13:58
28	4	((stress adj2 test$3) near4 ((integrated adj2 circuit) or IC$2)) and (reduc$5 near3 current)	USPAT; EPO; JPO; DERWENT	2004/01/15 14:00
29	35	(test$3 near2 ((integrated adj1 circuit) or IC$2)) same (reduc$5 near3 current)	USPAT; EPO; JPO; DERWENT	2004/01/15 14:01
30	421	(test$3 near2 ((integrated adj1 circuit) or IC$2)) and (reduc$5 near3 current)	USPAT; EPO; JPO; DERWENT	2004/01/15 14:01
31	75	(test$3 near2 ((integrated adj1 circuit) or IC$2)) and (reduc$5 near3 current) and flip-flop$1	USPAT; EPO; JPO; DERWENT	2004/01/15 14:02
32	163	(test$3 near2 ((integrated adj1 circuit) or IC$2)) and (reduc$5 near3 current) and (flip-flop$1 or latch$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 14:02
33	23	(test$3 near2 ((integrated adj1 circuit) or IC$2)) and (reduc$5 near3 current) and ((plurality or multiple) adj3 (flip-flop$1 or latch$3))	USPAT; EPO; JPO; DERWENT	2004/01/15 14:03
34	58	(test$3 near2 (circuit or IC$2)) and (reduc$5 near3 current) and ((plurality or multiple) adj3 (flip-flop$1 or latch$3))	USPAT; EPO; JPO; DERWENT	2004/01/15 14:26
35	7	(test$3 adj2 IC$2) and (reduc$5 near3 current) and ((plurality or multiple) adj3 (flip-flop$1 or latch$3))	USPAT; EPO; JPO; DERWENT	2004/01/15 14:26
36	8	(test$3 near2 IC$2) and (reduc$5 near3 current) and ((plurality or multiple) adj3 (flip-flop$1 or latch$3))	USPAT; EPO; JPO; DERWENT	2004/01/15 14:33
37	105	bernstein-k$.in.	USPAT; EPO; JPO; DERWENT	2004/01/15 14:37
39	13	bernstein-k$.in.and test$3	USPAT; EPO; JPO; DERWENT	2004/01/15 14:38
38	3	bernstein-k$.in.and stress$3	USPAT; EPO; JPO; DERWENT	2004/01/15 14:54
40	3	VDD0 and VDD1 and VDD2	USPAT; EPO; JPO; DERWENT	2004/01/15 15:00
41	14930	(first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))	USPAT; EPO; JPO; DERWENT	2004/01/15 15:01
42	1730	((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) and ((first adj2 logic) or (second adj3 logic))	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03
43	504	((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03
44	133	(((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))) and test$3	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03

45	10	(((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))) and test$3 and LSSD	USPAT; EPO; JPO; DERWENT	2004/01/15 15:49
46	26	(((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))) and (scan adj2 test$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 15:04
47	12	(((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))) and LSSD	USPAT; EPO; JPO; DERWENT	2004/01/15 15:50